ADICHUNCHANAGIRI UNIVERSITY

**18EC34**

**Third Semester BE Degree Examination January 2020**

**(CBCS Scheme)**

Time: 3 Hours Max Marks: 100 Marks

**Sub: Digital Electronics**

**Instructions:** 1. Answer five full questions.

2. Choose one full question from each module.

3. Your answer should be specific to the questions asked.

4. Write the same question numbers as they appear in this question paper.

5. Write Legibly.

**Module -1**

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| --- | --- | --- | --- | --- |
| 1 | a  | Define the following(i) Combinational logic (ii) Cannonical SOP (iii) Cannonical POS (iv) Incompletely specified functions | 4 | M |
|  | b | Obtain minimal expression using k-map for the following incompletely specified functionF(a,b,c,d)=∑m(0,1,4,6,7,9,15)+∑d(3,5,11,13) and draw the logic diagram using basic gates. | 8 | M |
|  | c | Design a combinational logic circuit which takes two, 2-bit binary numbers as its input and generates an output equal to 1, when the sum of the two number is odd. |  8 | M |
|  | Or |
| 2 | a | Simplify the given Boolean Function using Quine-Mcluskey methodY=ΠM(0,6,7,8,9,13)+Πdc(5,15) | 10 | M |
|  | b | Identify all prime implicants and essential prime implicants of the following function using k-map i) f(a,b,c,d)=∑m(6,7,9,10,13)+dc(1,4,5,11,15)ii) f(a,b,c,d)=ΠM(1,2,3,4,9,10)+dc(0,14,15) | 10 | M |

**Module -2**

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| 3 | a | Implement the following functions using 3:8 decoder(IC-74138) i) f1(a,b,c,d) = πM(2,4,5,7,9,10,13,14)ii) f2(a,b,c,d) = Σm(1,3,5,8,12,14,15) | 10 | M |
|  | b | What is Magnitude Comparator? Design 2 bit Comparator by writing Truth table, Expression and logic diagram. | 10 | M |
|  | Or |
| 4 | a | Design 16:1 multiplexer using 8:1 multiplexer. | 6 | M |
|  | b | Design a keypad interface to a digital system using ten line BCD encoder(74147). | 6 | M |
|  | c | Explain 4bit Carry look ahead Adder with neat diagram and relevant expressions. | 8 | M |

**Module -3**

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| 5 | a | Explain the Operation of a Switch debouncer built using SR latch with the help of circuits and waveforms. | 8 | M |
|  | b | Explain MS JK flip-flop with the help of circuit diagram and waveforms. | 8 | M |
|  | c | Explain the working Principle of 2 bit Ripple Binary Counter using the Edge Triggered JK Flip-flop. Also draw the Timing Diagram. | 4 | M |
|  | Or |
| 6 | a | Explain Positive Edge Triggered D Flip-flop with the help of circuit diagram and waveforms. | 8 | M |
|  | b | Describe the working of Universal Shift Register with the help of register operation and mode control table. | 8 | M |
|  | c | Obtain the Characteristic Equations for the following Flip-flops (i) JK (ii) D | 4 | M |

**Module -4**

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| 7 | a | Design a Synchronous Mod-6 counter usingSR flip-flop. | 10 | M |
|  | b | Analyze the following sequential circuit shown in Fig below and obtaini) Flip-flop input andoutputequation ii) Transitionequationiii)Transitiontable iv)State table v) Draw thestatediagram  | 10 | M |
|  | Or |
| 8 | a | Explain Mealy and Moore models of clocked synchronous sequential circuits with necessaryblockdiagrams. | 10 | M |
|  | b | Design a synchronous counter using JK flip flop to count the following sequence 7,4,3,1,6,0,7….. | 10 | M |

**Module -5**

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| --- | --- | --- | --- | --- |
| 9 | a | Explain the architecture of Field programmable gate array. | 10 | M |
|  | b | Implement i) Parallel adder with accumulator using CPLD ii) Shift register using FPGA. | 10 | M |
|  | Or |
| 10 | a | Design sequential circuits using ROM’s and PLA’s | 10 | M |
|  | b | Explain the concept of programmable logic array’s with suitable examples. | 10 | M |